

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: S. IKEDA, et al.

Serial No.: To be assigned

Filed: April 8, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR
MANUFACTURING THE SAME

Group: n/a

Examiner: n/a

LETTER

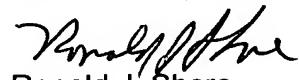
Assistant Commissioner for Patents
Washington, D.C. 20231

June 11, 1998

Sir:

Applicants reassert their claim for priority of Japanese Application No. 10-226663 filed on August 11, 1998.

Respectfully submitted,
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Enclosure